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Feb 202

	U		Inventor Δ	Document ID	Issue Date	Page	Title	Current OR	Current XRef	Ret Δ
1.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Faraone, Lorenzo	US 4757360 A	19880712	6	Floating gate memory device with facing asperities on floating and control gates	257/317	257/900; 257/E29 304	
2.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Lee, Jongho et al.	US 20020106536 A1	20020808	13	Dielectric layer for semiconductor device and method of manufacturing the same	428/702	428/428	
3.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Lee, Woo-Hyeong et al.	US 5923056 A	19990713	6	Electronic components with doped metal oxide dielectric materials and a process for making electronic components with doped metal oxide	257/192	257/410; 257/411	
4.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Muralidhar, Ramachandran et al.	US 6320784 B1	20011120	7	Memory cell and method for programming thereof	365/151	257/E29 301; 257/E29 308;	
5.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Nguyen, Bich-Yen et al.	US 20020137250 A1	20020926	10	High K dielectric film and method for making	438/53		
6.	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Uchida, Hidetsugu	US 6229175 B1	20010508	24	Nonvolatile memory	257/315	257/298; 257/316;	
7.	<input type="checkbox"/>	<input type="checkbox"/>	Ahn, Kie Y. et al.	US 20020130338 A1	20020919	9	Structures, methods, and systems for ferroelectric memory transistors	257/295		
8.	<input type="checkbox"/>	<input type="checkbox"/>	Ahn, Kie Y. et al.	US 20020086556 A1	20020704	11	Methods of forming silicon-doped aluminum oxide, and methods of forming transistors and memory devices	438/785		

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May 2003

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Drafts

BRS

BRS

BRS

BRS: (float\$3 adj gate) same (control adj gate)

BRS

BRS

Pending

Active

Failed

Saved

(1) 09/04/9877

(1813) tunnel adj barrier

(5) low adj (tunnel adj barrier)

(109489) asymmetri\$4

(0) asymmetri\$4 adj (low adj (tunnel adj barrier))

(12792) (float\$3 adj gate) same (control adj gate)

(12792) (float\$3 adj gate) same (control adj gate)

USPAT:US PGPUB: EPO: JPO: DERWENT: ISM: TDB

Default operator: OR

"6210999" "6541280".pn

Plurals

Highlight all hit terms initially

Nov 2003

	U	Inventor s	Document ID	Issue Date	Page	Title	Current OR	Current XRef
1	<input checked="" type="checkbox"/>	Gardner, Mark L et al.	US 6210999 B1	20010403	14	Method and test structure for low-temperature integration of high dielectric constant gate dielectrics into self-aligned semiconductor devices	438/183	257/332;
2	<input checked="" type="checkbox"/>	Kaushik, Vidya S. et al.	US 6541280 B2	20030401	8	High K dielectric film	438/3	257/E21.208;
3	<input type="checkbox"/>	GARDNER, M L et al.	US 6210999 B	20010403		Semiconductor device for fabricating MOS IC, comprises gate dielectric having high dielectric constant and gate conductor laid one above another sequentially in trench formed a		361/311;
4	<input type="checkbox"/>	KAUSHIK, V S et al.	US 20020137317 A	20030401	8	Semiconductor structure for semiconductor devices, has gate dielectric layer containing lanthanum, aluminum and oxygen, and electrode layer, formed on semiconductor substrate		

Ready

26/04